CLAIMS

1. An integrated semiconductor device, comprising:

a semiconductor material substrate;

a polysilicon line, said polysilicon line having micro-rough indentations on top surface portion of the polysilicon line; and

a silicide film covering said micro-rough top surface portion of the polysilicon line.

2. The integrated device of claim 1, further comprising:

a plurality of isolation areas;

a thin oxide film between said polysilicon line and the substrate; and

a plurality of patterned active regions positioned on the substrate and on opposite sides of said polysilicon line.

3. The integrated device of claim 2 wherein said polysilicon line forms a polysilicon gate region of the device and said active regions are source and drain regions of the device.

4. The integrated device of claim 3, further comprising spacers adjacent to the polysilicon gate region and lightly doped regions under said spacers and adjacent to said source and drain regions.

5. The integrated device of claim 1 wherein said silicide film comprises titanium silicide or titanium silicide/titanium nitride stack film.

6. The integrated device of claim 1 wherein said silicide film covering said micro-rough top surface of the polysilicon line has an increased effective surface area.

7. The integrated device of claim 1, further comprising a metallization structure positioned on the silicide film for providing interconnection.

8. The integrated device of claim 7 wherein said metallization structure comprises a multi-stack metal layer.